Abstract of the Disclosure:

A ferroelectric transistor suitable as a memory element has a first gate intermediate layer and a first gate electrode disposed on the surface of a semiconductor substrate and disposed between source/drain regions. The first gate intermediate layer contains at least one ferroelectric layer. In addition to the first gate intermediate layer, a second gate intermediate layer and a second gate electrode are configured between the source/drain regions. The second gate intermediate layer contains a dielectric layer. The first gate electrode and the second gate electrode are connected to each other via a diode structure.

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